What is claimed is :

1. A channel region of a depletion type lateral field effect transistor, said channel region of a first conductivity type being selectively provided in a semiconductor region of a second conductivity type, and said channel region underlying a gate insulating film,

wherein an interface of said channel region to said gate insulating film lies at a lower level than an upper surface of said semiconductor region.

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2. The channel region as claimed in claim 1, wherein said semiconductor region comprises a well region selectively provided in a semiconductor substrate.

3. The channel region as claimed in claim 1, wherein said channel region comprises a diffusion layer doped with an impurity of said first conductivity type which is for adjustment to a threshold voltage of said depletion type lateral field effect transistor.

4. A well region for a depletion type lateral field effect transistor, said well region of a second conductivity type being selectively provided in a semiconductor substrate, said well region having an upper surface and including an impurity diffused region which is selectively provided in said well region, and said impurity diffused region being doped with an

impurity of a first conductivity type which is for adjustment to a threshold voltage of said depletion type lateral field effect transistor,

wherein said upper surface of said impurity diffused region lies at a lower level than said upper surface of said well region.

5. The well region as claimed in claim 1, wherein said upper surface of said impurity diffused region is bounded with a gate insulating film.

6. The well region as claimed in claim 1, wherein said impurity diffused region forms a channel layer of said depletion type lateral field effect transistor.

6. A semiconductor wafer comprising :

a semiconductor substrate of a first conductivity type ;

an epitaxial layer of the first conductivity type overlying said semiconductor substrate ;

a well region of a second conductivity type selectively provided in said epitaxial layer ; and

an impurity diffused channel region being selectively provided in said well region, and said impurity diffused channel region being doped with an impurity of the first conductivity type which is for adjustment to a threshold voltage of a depletion type lateral field effect transistor,

wherein said upper surface of said impurity diffused channel

region lies at a lower level than said upper surface of said well region.

7. The semiconductor wafer as claimed in claim 6, wherein said upper surface of said impurity diffused region is bounded with a gate insulating film.

8. A depletion type lateral MOS field effect transistor comprising :

a channel region of a first conductivity type being selectively provided in a semiconductor region of a second conductivity type ;

source and drain regions of the first conductivity type being selectively provided in said semiconductor region, said channel region being interposed between said source and drain regions ;

a gate insulating film extending over said channel region ; and

a gate electrode provided on said gate insulating film,

wherein an interface of said channel region to said gate insulating film lies at a lower level than an upper surface of said semiconductor region.

9. The channel region as claimed in claim 8, wherein said semiconductor region comprises a well region selectively provided in an epitaxial layer of the first conductivity type, and said epitaxial layer overlying a semiconductor substrate of the first conductivity type.

10. The channel region as claimed in claim 8, wherein said channel

region comprises a diffusion layer doped with an impurity of said first conductivity type which is for adjustment to a threshold voltage of said depletion type lateral field effect transistor.

11. A semiconductor wafer including :

an impurity diffused region of a first conductivity type being selectively provided in a semiconductor region of a second conductivity type ; and

an oxide film overlying said impurity diffused region,

wherein an interface of said impurity diffused region to said oxide film lies at a lower level than an upper surface of said semiconductor wafer.

12. The semiconductor wafer as claimed in claim 11, wherein said semiconductor region comprises a well region selectively provided in a semiconductor substrate.

13. The semiconductor wafer as claimed in claim 11, wherein said channel region comprises a diffusion layer doped with an impurity of said first conductivity type which is for adjustment to a threshold voltage of a depletion type lateral field effect transistor.

14. The semiconductor wafer as claimed in claim 11, wherein said oxide film has a thickness of at least 5000 angstroms.

15. A method of forming a channel region of a depletion type lateral field effect transistor, comprising the steps of :

selectively forming a channel region of a first conductivity type in a semiconductor region of a second conductivity type ;

subjecting an upper region of said channel region to a selective oxidation to form an oxide film which overlies said channel region,

wherein an interface of said impurity diffused region to said oxide film lies at a lower level than an upper surface of said semiconductor wafer.

16. The method as claimed in claim 15, wherein said oxide film has a thickness of at least 5000 angstroms.

17. The method as claimed in claim 15, wherein said semiconductor region comprises a well region selectively formed in an epitaxial layer over a semiconductor substrate.

18. The method as claimed in claim 15, wherein said channel region comprises a diffusion layer doped with an impurity of said first conductivity type which is for adjustment to a threshold voltage of a depletion type lateral field effect transistor.

19. The method as claimed in claim 15, wherein said oxidation is a

wet oxidation.

20. The method as claimed in claim 15, wherein said oxide film overlying said channel region is formed at the same time of forming at least a field oxide film.

21. A method of forming a channel region of a depletion type lateral field effect transistor, comprising the steps of :

selectively introducing a first impurity of a second conductivity type at a first impurity concentration into a first selected region of a semiconductor region of a first conductivity type ;

selectively introducing a second impurity of the first conductivity type at a second impurity concentration into a second selected region in said first selected region, said second impurity concentration being higher than said first impurity concentration ;

carrying out a heat treatment for activating said first and second impurities to form a well region on said first selected region and a channel region on said second selected region concurrently ; and

subjecting an upper region of said channel region to a selective oxidation to form an oxide film which overlies said channel region,

so that an interface of said impurity diffused region to said oxide film lies at a lower level than an upper surface of said semiconductor wafer.

22. The method as claimed in claim 21, wherein said oxide film has a

thickness of at least 5000 angstroms.

23. The method as claimed in claim 21, wherein said semiconductor region comprises a well region selectively formed in an epitaxial layer over a semiconductor substrate.

24. The method as claimed in claim 21, wherein said channel region comprises a diffusion layer doped with an impurity of said first conductivity type which is for adjustment to a threshold voltage of a depletion type lateral field effect transistor.

25. The method as claimed in claim 21, wherein said oxidation is a wet oxidation.

26. The method as claimed in claim 21, wherein said oxide film overlying said channel region is formed at the same time of forming at least a field oxide film.

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